Touch Screen Digitizer

AD7843

FEATURES

4-wire touch screen interface
Specified throughput rate of 125 kSPS
Low power consumption:
1.37 mW max at 125 kSPS with V_{CC} = 3.6 V
Single supply, V_{CC} of 2.2 V to 5.25 V
Ratiometric conversion
High speed serial interface
Programmable 8-bit or 12-bit resolution
2 auxiliary analog inputs
Shutdown mode: 1 µA max
16-lead QSOP and TSSOP packages

APPLICATIONS

Personal digital assistants
Smart hand-held devices
Touch screen monitors
Point-of-sales terminals
Pagers

FUNCTIONAL BLOCK DIAGRAM

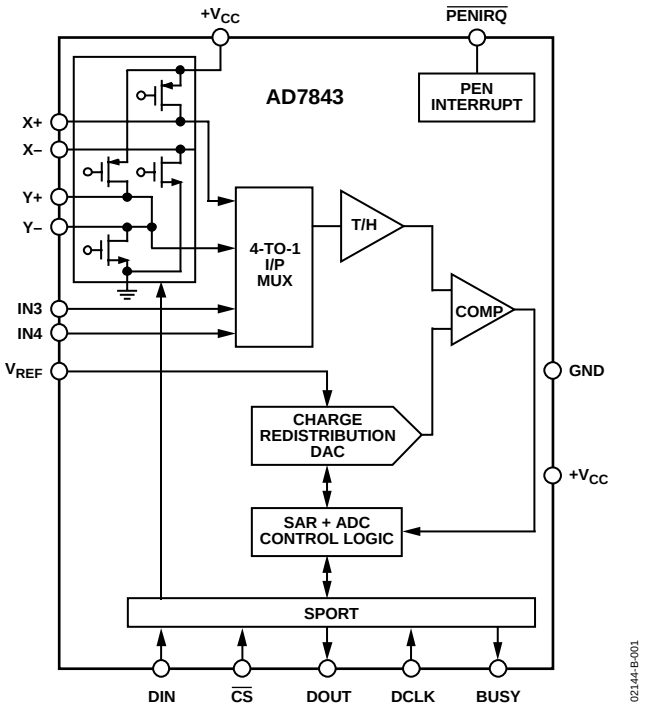


Figure 1.

GENERAL DESCRIPTION

The AD7843 is a 12-bit successive approximation ADC with a synchronous serial interface and low on resistance switches for driving touch screens. The part operates from a single 2.2 V to 5.25 V power supply and features throughput rates greater than 125 kSPS.

The external reference applied to the AD7843 can be varied from 1 V to +V_{CC}, while the analog input range is from 0 V to V_{REF}. The device includes a shutdown mode that reduces the current consumption to less than 1 µA.

The AD7843 features on-board switches. This, coupled with low power and high speed operation, make this device ideal for battery-powered systems such as personal digital assistants with resistive touch screens, and other portable equipment. The part is available in a 16-lead 0.15" quarter size outline package (QSOP) and a 16-lead thin shrink small outline package (TSSOP).

PRODUCT HIGHLIGHTS

1. Ratiometric conversion mode available eliminating errors due to on-board switch resistances.
2. Maximum current consumption of 380 µA while operating at 125 kSPS.
3. Power-down options available.
4. Analog input range from 0 V to V_{REF}.
5. Versatile serial I/O port.

Rev. B

One Technology Way, P.O. Box 9106, Norwood, MA 02062-9106, U.S.A.
Tel: 781.329.4700 **www.analog.com**
Fax: 781.326.8703

TABLE OF CONTENTS

REVISION HISTORY

3/04—Data Sheet Changed from Rev. A to Rev. B

Updated Format ... Universal
Changes to Absolute Maximum Ratings ... 5
Addition to the PD0 and PD1 Section ... 14
Additions to Ordering Guide ... 20

3/03—Data Sheet Changed from Rev. 0 to Rev. A

Updated Outline Dimensions ... 16

SPECIFICATIONS

V_{CC} = 2.7 V to 3.6 V, V_{REF} = 2.5 V, f_{SCLK} = 2 MHz, T_A = −40°C to +85°C, unless otherwise noted.

Table 1.

Parameter	AD7843A[1]	Unit	Test Conditions/Comments
DC ACCURACY			
Resolution	12	Bits	
No Missing Codes	11	Bits min	
Integral Nonlinearity[2]	±2	LSB max	
Offset Error[2]	±6	LSB max	V_{CC} = 2.7 V
Offset Error Match[3]	1	LSB max	
	0.1	LSB typ	
Gain Error[2]	±4	LSB max	
Gain Error Match[3]	1	LSB max	
	0.1	LSB typ	
Power Supply Rejection	70	dB typ	
SWITCH DRIVERS			
On-Resistance[2]			
Y+, X+	5	Ω typ	
Y−, X−	6	Ω typ	
ANALOG INPUT			
Input Voltage Ranges	0 to V_{REF}	V	
DC Leakage Current	±0.1	µA typ	
Input Capacitance	37	pF typ	
REFERENCE INPUT			
V_{REF} Input Voltage Range	1.0/+V_{CC}	V min/max	
DC Leakage Current	±1	µA max	
V_{REF} Input Impedance	5	GΩ typ	$\overline{CS}$ = GND or +V_{CC}
V_{REF} Input Current[3]	20	µA max	8 µA typ
	1	µA typ	f_{SAMPLE} = 12.5 kHz
	1	µA max	$\overline{CS}$ = +V_{CC}; 0.001 µA typ
LOGIC INPUTS			
Input High Voltage, V_{INH}	2.4	V min	
Input Low Voltage, V_{INL}	0.4	V max	
Input Current, I_{IN}	±1	µA max	Typically 10 nA, V_{IN} = 0 V or +V_{CC}
Input Capacitance, C_{IN}[4]	10	pF max	
LOGIC OUTPUTS			
Output High Voltage, V_{OH}	V_{CC} − 0.2	V min	I_{SOURCE} = 250 µA; V_{CC} = 2.2 V to 5.25 V
Output Low Voltage, V_{OL}	0.4	V max	I_{SINK} = 250 µA
$\overline{PENIRQ}$ Output Low Voltage, V_{OL}	0.4	V max	I_{SINK} = 250 µA; 100 kW pull-up
Floating-State Leakage Current	±10	µA max	
Floating-State Output Capacitance[4]	10	pF max	
Output Coding	Straight (Natural) Binary		
CONVERSION RATE			
Conversion Time	12	DCLK Cycles max	
Track-and-Hold Acquisition Time	3	DCLK Cycles min	
Throughput Rate	125	kSPS max	

Footnotes on next page.

Parameter	AD7843A[1]	Unit	Test Conditions/Comments
POWER REQUIREMENTS			
V_{CC} (Specified Performance)	2.7/3.6	V min/max	Functional from 2.2 V to 5.25 V
I_{CC}[5]			Digital I/Ps = 0 V or V_{CC}
Normal Mode (f_{SAMPLE} = 125 kSPS)	380	µA max	V_{CC} = 3.6 V, 240 µA typ
Normal Mode (f_{SAMPLE} = 12.5 kSPS)	170	µA typ	V_{CC} = 2.7 V, f_{DCLK} = 200 kHz
Normal Mode (Static)	150	µA typ	V_{CC} = 3.6 V
Shutdown Mode (Static)	1	µA max	
Power Dissipation[5]			
Normal Mode (f_{SAMPLE} = 125 kSPS)	1.368	mW max	V_{CC} = 3.6 V
Shutdown	3.6	µW max	V_{CC} = 3.6 V

[1] Temperature range as follows: A Version: −40°C to +85°C.
[2] See the Terminology section.
[3] Guaranteed by design.
[4] Sample tested @ 25°C to ensure compliance.
[5] See the Power vs. Throughput Rate section.

TIMING SPECIFICATIONS

$T_A = T_{MIN}$ to T_{MAX}, unless otherwise noted; V_{CC} = 2.7 V to 3.6 V, V_{REF} = 2.5 V.

Table 2. Timing Specifications[1]

Parameter	Limit at T_{MIN}, T_{MAX}	Unit	Description
f_{DCLK}[2]	10	kHz min	
	2	MHz max	
t_{ACQ}	1.5	µs min	Acquisition time
t_1	10	ns min	$\overline{CS}$ falling edge to First DCLK rising edge
t_2	60	ns max	$\overline{CS}$ falling edge to BUSY three-state disabled
t_3	60	ns max	$\overline{CS}$ falling edge to DOUT three-state disabled
t_4	200	ns min	DCLK high pulse width
t_5	200	ns min	DCLK low pulse width
t_6	60	ns max	DCLK falling edge to BUSY rising edge
t_7	10	ns min	Data setup time prior to DCLK rising edge
t_8	10	ns min	Data valid to DCLK hold time
t_9[3]	200	ns max	Data access time after DCLK falling edge
t_{10}	0	ns min	$\overline{CS}$ rising edge to DCLK ignored
t_{11}	200	ns max	$\overline{CS}$ rising edge to BUSY high impedance
t_{12}[4]	200	ns max	$\overline{CS}$ rising edge to DOUT high impedance

[1] Sample tested at 25°C to ensure compliance. All input signals are specified with tr = tf = 5 ns (10% to 90% of V_{CC}) and are timed from a voltage level of 1.6 V.
[2] Mark/space ratio for the SCLK input is 40/60 to 60/40.
[3] Measured with the load circuit in Figure 2 and defined as the time required for the output to cross 0.4 V or 2.0 V.
[4] t_{12} is derived from the measured time taken by the data outputs to change 0.5 V when loaded with the circuit in Figure 2. The measured number is then extrapolated back to remove the effects of charging or discharging the 50 pF capacitor. This means that the time, t_{12}, quoted in the timing characteristics is the true bus relinquish time of the part and is independent of the bus loading.

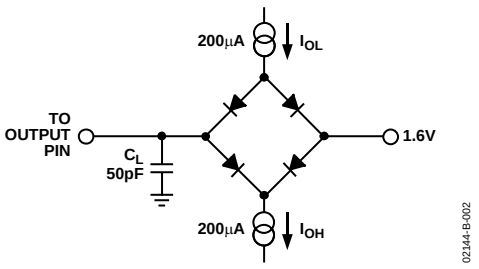


Figure 2. Load Circuit for Digital Output Timing Specifications

ABSOLUTE MAXIMUM RATINGS

T_A = 25°C, unless otherwise noted.

Table 3.

Parameter	Rating
+V_{CC} to GND	−0.3 V to +7 V
Analog Input Voltage to GND	−0.3 V to V_{CC} + 0.3 V
Digital Input Voltage to GND	−0.3 V to V_{CC} + 0.3 V
Digital Output Voltage to GND	−0.3 V to V_{CC} + 0.3 V
V_{REF} to GND	−0.3 V to V_{CC} + 0.3 V
Input Current to Any Pin Except Supplies[1]	±10 mA
Operating Temperature Range	
Commercial	−40°C to +85°C
Storage Temperature Range	−65°C to +150°C
Junction Temperature	150°C
QSOP, TSSOP Package, Power Dissipation	450 mW
θ_{JA} Thermal Impedance	149.97°C/W (QSOP)
	150.4°C/W (TSSOP)
θ_{JC} Thermal Impedance	38.8°C/W (QSOP)
	27.6°C/W (TSSOP)
IR Reflow Soldering	
Peak Temperture	220°C (±5°C)
Time-to-Peak Temperture	10 sec to 30 sec
Ramp-Down Rate	6°C/sec max
Pb-free parts only	
Peak Temperture	250°C
Time-to-Peak Temperture	20 sec to 40 sec
Ramp-Up Rate	3°C/sec max
Ramp-Down Rate	6°C/sec max

[1] Transient currents of up to 100 mA do not cause SCR latch-up.

Stresses above those listed under Absolute Maximum Rating may cause permanent damage to the device. This is a stress rating only; functional operation of the device at these or any other conditions above those listed in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

ESD CAUTION

ESD (electrostatic discharge) sensitive device. Electrostatic charges as high as 4000 V readily accumulate on the human body and test equipment and can discharge without detection. Although this product features proprietary ESD protection circuitry, permanent damage may occur on devices subjected to high energy electrostatic discharges. Therefore, proper ESD precautions are recommended to avoid performance degradation or loss of functionality.

PIN CONFIGURATION AND FUNCTION DESCRIPTIONS

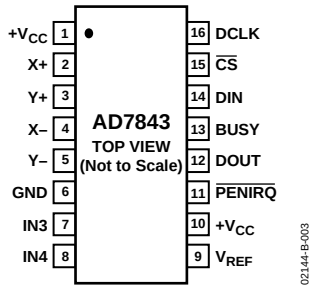


Figure 3. Pin Configuration QSOP/TSSOP

Table 4. Pin Function Descriptions

Pin No.	Mnemonic	Function
1, 10	$+V_{CC}$	Power Supply Input. The $+V_{CC}$ range for the AD7843 is from 2.2 V to 5.25 V. Both $+V_{CC}$ pins should be connected directly together.
2	X+	X+ Position Input. ADC Input Channel 1.
3	Y+	Y+ Position Input. ADC Input Channel 2.
4	X–	X– Position Input.
5	Y–	Y– Position Input.
6	GND	Analog Ground. Ground reference point for all circuitry on the AD7843. All analog input signals and any external reference signal should be referred to this GND voltage.
7	IN3	Auxiliary Input 1. ADC Input Channel 3.
8	IN4	Auxiliary Input 2. ADC Input Channel 4.
9	V_{REF}	Reference Input for the AD7843. An external reference must be applied to this input. The voltage range for the external reference is 1.0 V to $+V_{CC}$. For specified performance, it is 2.5 V.
11	$\overline{\text{PENIRQ}}$	Pen Interrupt. CMOS logic open-drain output (requires 10 kΩ to 100 kΩ pull-up register externally).
12	DOUT	Data Out. Logic Output. The conversion result from the AD7843 is provided on this output as a serial data stream. The bits are clocked out on the falling edge of the DCLK input. This output is high impedance when $\overline{CS}$ is high.
13	BUSY	BUSY Output. Logic Output. This output is high impedance when $\overline{CS}$ is high.
14	DIN	Data In. Logic input. Data to be written to the AD7843 control register is provided on this input and is clocked into the register on the rising edge of DCLK (see the Control Register section).
15	$\overline{CS}$	Chip Select Input. Active Low Logic Input. This input provides the dual function of initiating conversions on the AD7843 and also enables the serial input/output register.
16	DCLK	External Clock Input. Logic Input. DCLK provides the serial clock for accessing data from the part. This clock input is also used as the clock source for the AD7843 conversion process.

TERMINOLOGY

Integral Nonlinearity
This is the maximum deviation from a straight line passing through the endpoints of the ADC transfer function. The endpoints of the transfer function are zero scale, a point 1 LSB below the first code transition, and full scale, a point 1 LSB above the last code transition.

Differential Nonlinearity
This is the difference between the measured and the ideal 1 LSB change between any two adjacent codes in the ADC.

Offset Error
This is the deviation of the first code transition (00…000) to (00…001) from the ideal, that is, AGND + 1 LSB.

Gain Error
This is the deviation of the last code transition (111…110) to (111…111) from the ideal (V_{REF} − 1 LSB) after the offset error has been adjusted out.

Track-and-Hold Acquisition Time
The track-and-hold amplifier enters the acquisition phase on the fifth falling edge of DCLK after the START bit has been detected. Three DCLK cycles are allowed for the track-and-hold acquisition time. The input signal is fully acquired to the 12-bit level within this time even with the maximum specified DCLK frequency. See the Analog Input section for more details.

On Resistance
This is a measure of the ohmic resistance between the drain and source of the switch drivers.

TYPICAL PERFORMANCE CHARACTERISTICS

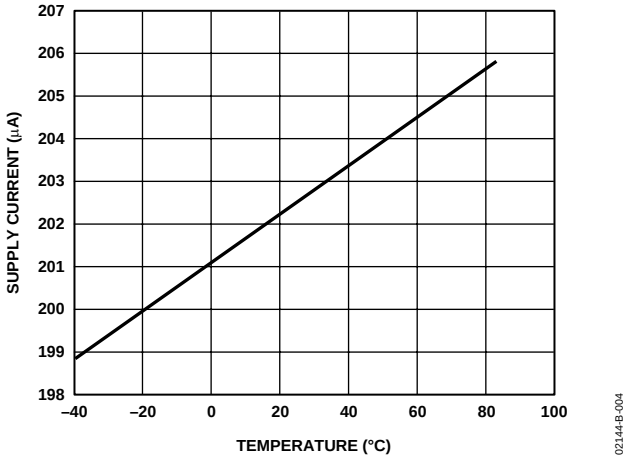


Figure 4. Supply Current vs. Temperature

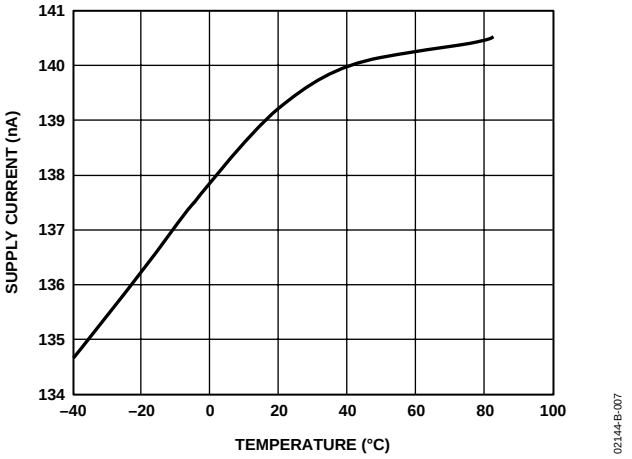


Figure 7. Power-Down Supply Current vs. Temperature

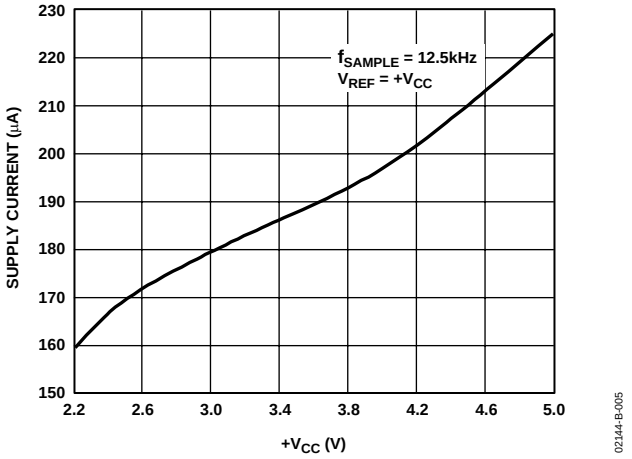


Figure 5. Supply Current vs. $+V_{CC}$

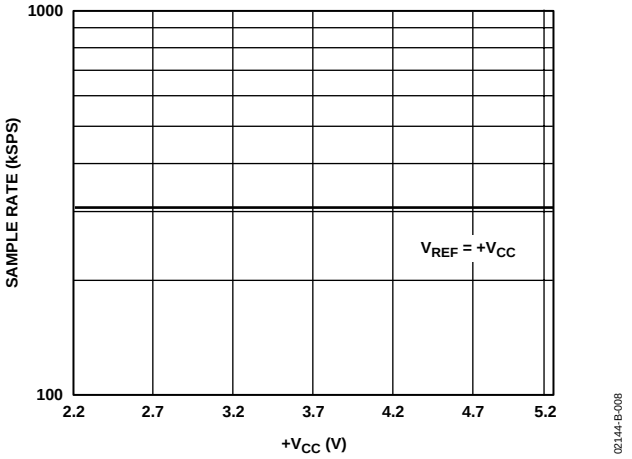


Figure 8. Maximum Sample Rate vs. $+V_{CC}$

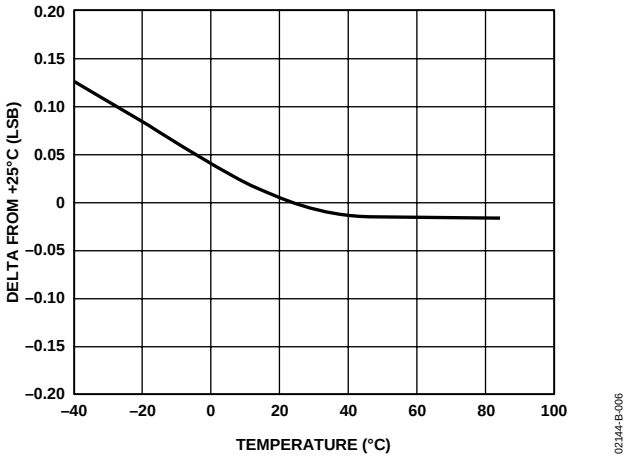


Figure 6. Change in Gain vs. Temperature

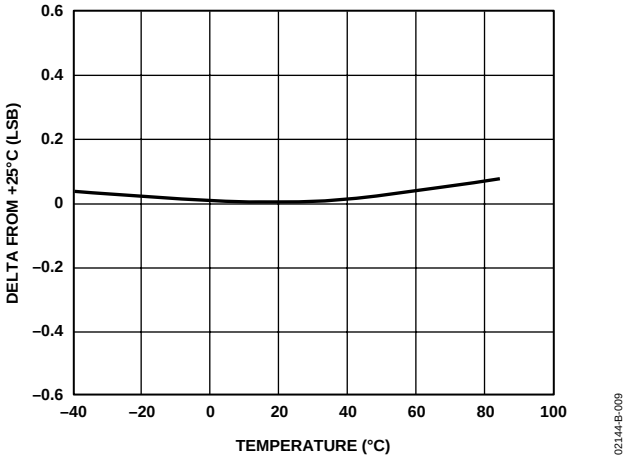


Figure 9. Change in Offset vs. Temperature

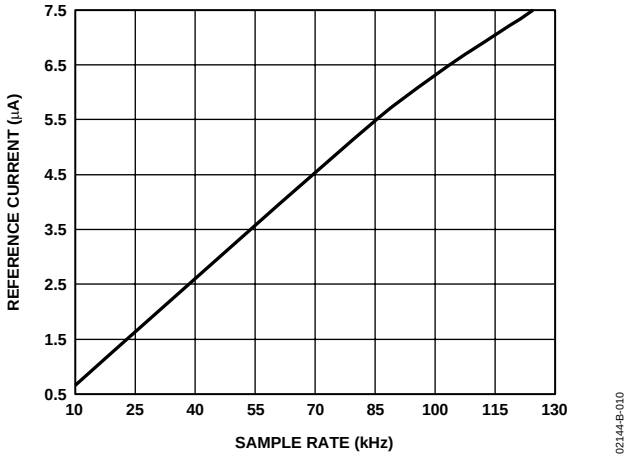


Figure 10. Reference Current vs. Sample Rate

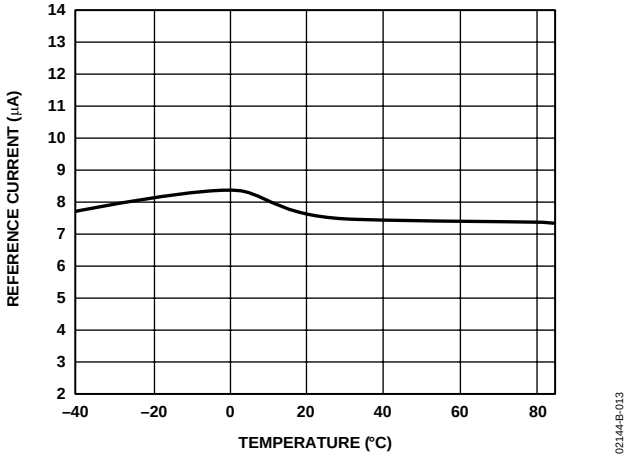


Figure 13. Reference Current vs. Temperature

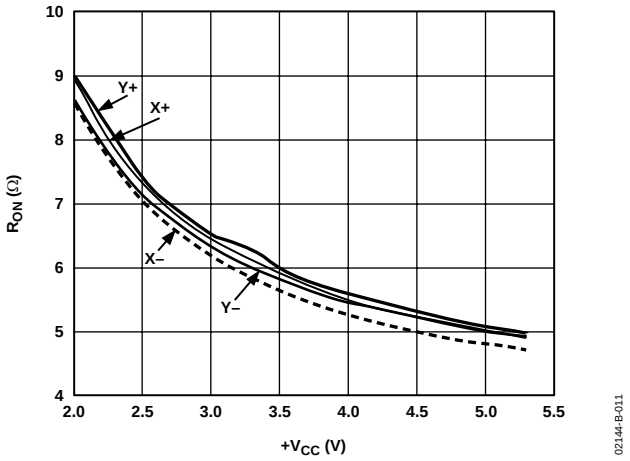


Figure 11. Switch-On Resistance vs. $+V_{CC}$
(X+, Y+: $+V_{CC}$ to Pin; X–, Y–: Pin to GND)

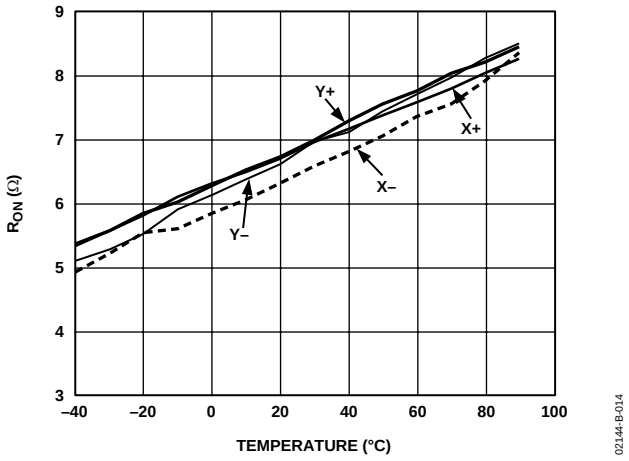


Figure 14. Switch-On Resistance vs. Temperature
(X+, Y+:$+V_{CC}$ to Pin; X–, Y–: Pin to GND)

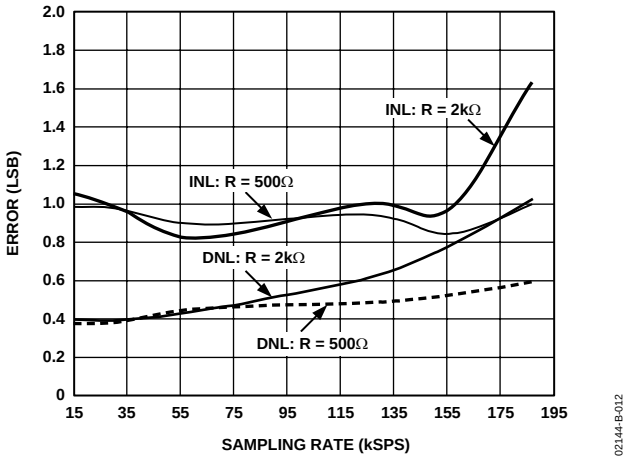


Figure 12. Maximum Sampling Rate vs. R_{IN}

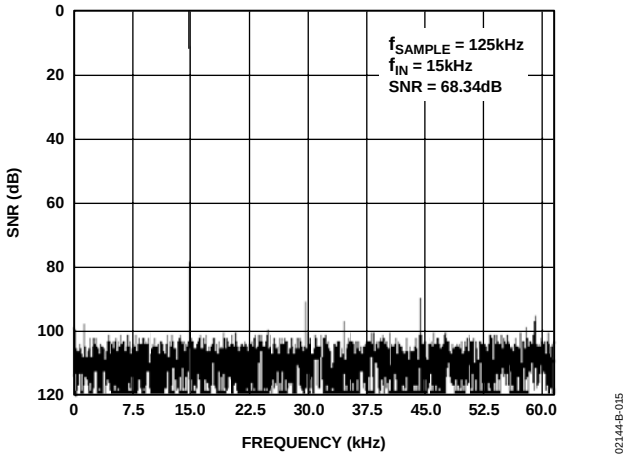


Figure 15. Auxiliary Channel Dynamic Performance
(f_{SAMPLE} =125 kHz, f_{INPUT} = 15 kHz)

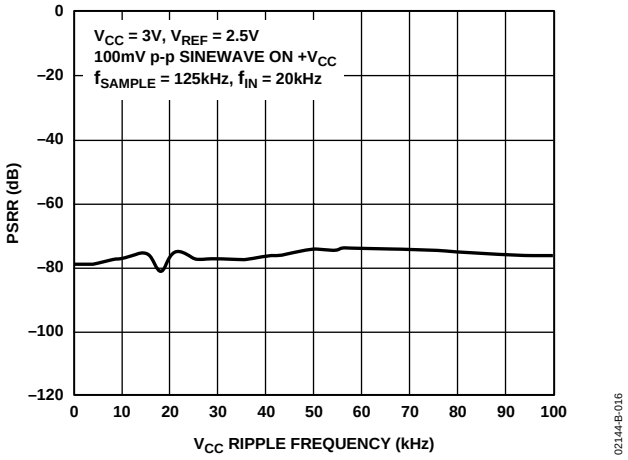


Figure 16. AC PSRR vs. Supply Ripple Frequency

Figure 16 shows the power supply rejection ratio versus V_{CC} supply frequency for the AD7843. The power supply rejection ratio is defined as the ratio of the power in the ADC output at full-scale frequency f_S to the power of a 100 mV sine wave applied to the ADC V_{CC} supply of frequency f_S:

$$PSRR \text{ (dB)} = 10 \log (Pf/Pfs)$$

where:

Pf is the power at frequency f in ADC output.
Pfs is the power at frequency f_S coupled onto the ADC V_{CC} supply.

Here a 100 mV p-p sine wave is coupled onto the V_{CC} supply. Decoupling capacitors of 10 μF and 0.1 μF were used on the supply.

CIRCUIT INFORMATION

The AD7843 is a fast, low-power, 12-bit, single-supply, A/D converter. The AD7843 can be operated from a 2.2 V to 5.25 V supply. When operated from either a 5 V supply or a 3 V supply, the AD7843 is capable of throughput rates of 125 kSPS when provided with a 2 MHz clock.

The AD7843 provides the user with an on-chip track-and-hold, multiplexer, ADC, and serial interface housed in tiny 16-lead QSOP or TSSOP packages, which offer the user considerable space-saving advantages over alternative solutions. The serial clock input (DCLK) accesses data from the part and also provides the clock source for the successive approximation ADC. The analog input range is 0 V to V_{REF} (where the externally-applied V_{REF} can be between 1 V and V_{CC}).

The analog input to the ADC is provided via an on-chip multiplexer. This analog input can be any one of the X and Y panel coordinates. The multiplexer is configured with low resistance switches that allow an unselected ADC input channel to provide power and an accompanying pin to provide ground for an external device. For some measurements, the on resistance of the switches could present a source of error. However, with a differential input to the converter and a differential reference architecture, this error can be negated.

ADC TRANSFER FUNCTION

The output coding of the AD7843 is straight binary. The designed code transitions occur at successive integer LSB values (that is, 1 LSB, 2 LSBs, and so forth.). The LSB size equals $V_{REF}/4096$. The ideal transfer characteristic for the AD7843 is shown in Figure 17.

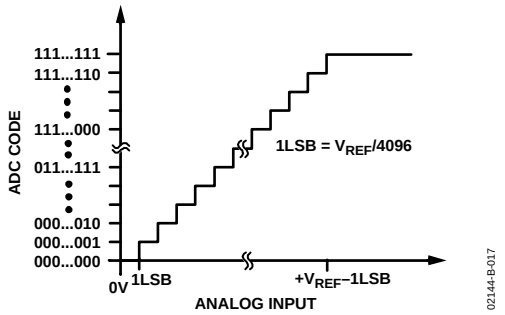


Figure 17. AD7843 Transfer Characteristic

TYPICAL CONNECTION DIAGRAM

Figure 18 shows a typical connection diagram for the AD7843 in a touch screen control application. The AD7843 requires an external reference and an external clock. The external reference can be any voltage between 1 V and V_{CC}. The value of the reference voltage sets the input range of the converter. The conversion result is output MSB first, followed by the remaining 11 bits and three trailing zeroes, depending on the number of clocks used per conversion. (See the Serial Interface section.) For applications where power consumption is a concern, the power management option should be used to improve power performance. See Table 7 for the available power management options.

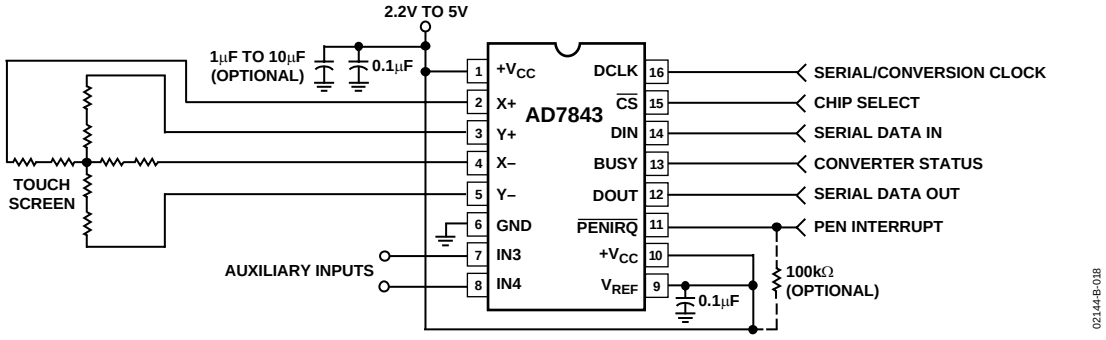


Figure 18. Typical Application Circuit

ANALOG INPUT

Figure 19 shows an equivalent circuit of the analog input structure of the AD7843, which contains a block diagram of the input multiplexer, the differential input of the ADC, and the differential reference.

Table 5 shows the multiplexer address corresponding to each analog input, both for the SER/$\overline{\text{DFR}}$ bit in the control register set high and low. The control bits are provided serially to the device via the DIN pin. For more information on the control register, see the Control Register section.

When the converter enters hold mode, the voltage difference between the +IN and –IN inputs (see Figure 19) is captured on the internal capacitor array. The input current on the analog inputs depends on the conversion rate of the device. During the sample period, the source must charge the internal sampling capacitor (typically 37 pF). Once the capacitor is fully charged, there is no further input current. The rate of charge transfer from the analog source to the converter is a function of conversion rate.

Acquisition Time

The track-and-hold amplifier enters tracking mode on the falling edge of the fifth DCLK after the START bit us detected (see Figure 24). The time required for the track-and-hold amplifier to acquire an input signal depends on how quickly the 37 pF input capacitance is charged. With zero source impedance on the analog input, three DCLK cycles are always sufficient to acquire the signal to the 12-bit level. With a source impedance R_{IN} on the analog input, the actual acquisition time required is calculated using the formula:

$$t_{ACQ} = 8.4 \times (R_{IN} + 100\ \Omega) \times 37\ \text{pF}$$

where R_{IN} is the source impedance of the input signal and 100 Ω and 37 pF is the input RC value. Depending on the frequency of DCLK used, three DCLK cycles may or may not be sufficient to acquire the analog input signal with various source impedance values.

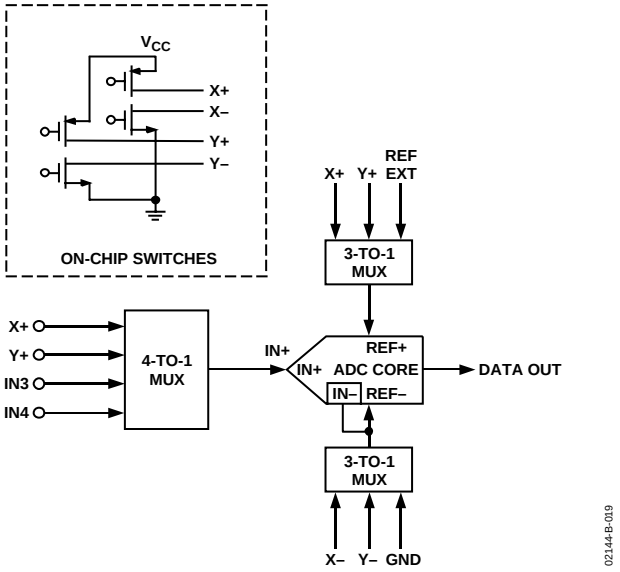


Figure 19. Equivalent Analog Input Circuit

Table 5. Analog Input, Reference, and Touch Screen Control

A2[1]	A1[1]	A0[1]	SER/$\overline{\text{DFR}}$	Analog Input	X Switches	Y Switches	+REF[2]	–REF[2]
0	0	1	1	X+	OFF	ON	V_{REF}	GND
0	1	0	1	IN3	OFF	OFF	V_{REF}	GND
1	0	1	1	Y+	ON	OFF	V_{REF}	GND
1	1	0	1	IN4	OFF	OFF	V_{REF}	GND
0	0	1	0	X+	OFF	ON	Y+	Y–
1	0	1	0	Y+	ON	OFF	X+	X–
1	1	0	0	Outputs Identity Code, 1000 0000 0000				

[1] All remaining configurations are invalid addresses.
[2] Internal node – not directly accessible by the user.

Touch Screen Settling

In some applications, external capacitors could be required across the touch screen to filter noise associated with it, for example, noise generated by the LCD panel or backlight circuitry. The value of these capacitors causes a settling time requirement when the panel is touched. The settling time typically appears as a gain error. There are several methods for minimizing or eliminating this issue. The problem could be that the input signal, reference, or both have not settled to their final value before the sampling instant of the ADC. Additionally, the reference voltage could still be changing during the conversion cycle. One option is to stop, or slow down the DCLK for the required touch screen settling time. This allows the input and reference to stabilize for the acquisition time, which resolves the issue for both single-ended and differential modes.

The other option is to operate the AD7843 in differential mode only for the touch screen and to program the AD7843 to keep the touch screen drivers on and not go into power-down (PD0 = PD1 = 1). Several conversions might be required, depending on the settling time required and the AD7843 data rate. Once the required number of conversions are made, the AD7843 can then be placed into a power-down state on the last measurement. The last method is to use the 15 DCLK cycle mode, which maintains the touch screen drivers on until it is commanded to stop by the processor.

Reference Input

The voltage difference between +REF and −REF (see Figure 19) sets the analog input range. The AD7843 operates with a reference input in the range of 1 V to V_{CC}. The voltage into the V_{REF} input is not buffered and directly drives the capacitor DAC portion of the AD7843. Figure 20 shows the reference input circuitry. Typically, the input current is 8 μA with V_{REF} = 2.5 V and f_{SAMPLE} = 125 kHz. This value varies by a few microamps, depending on the result of the conversion. The reference current diminishes directly with both conversion rate and reference voltage. As the current from the reference is drawn on each bit decision, clocking the converter more quickly during a given conversion period does not reduce the overall current drain from the reference.

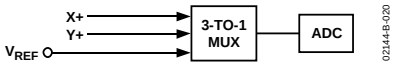


Figure 20. Reference Input Circuitry

When making touch screen measurements, conversions can be made in the differential (ratiometric) mode or the single-ended mode. If the SER/$\overline{DFR}$ bit is set to 1 in the control register, a single-ended conversion is performed. Figure 21 shows the configuration for a single-ended Y-coordinate measurement. The X+ input is connected to the analog to digital converter, the Y+ and Y− drivers are turned on, and the voltage on X+ is digitized. The conversion is performed with the ADC referenced from GND to V_{REF}. The advantage of this mode is that the switches that supply the external touch screen can be turned off once the acquisition is complete, resulting in a power saving. However, the on resistance of the Y drivers affects the input voltage that can be acquired. The full touch screen resistance may be in the order of 200 Ω to 900 Ω, depending on the manufacturer. Therefore if the on resistance of the switches is approximately 6 Ω, true full-scale and zero-scale voltages cannot be acquired regardless of where the pen/stylus is on the touch screen. Note that the minimum touch screen resistance recommended for use with the AD7843 is approximately 70 Ω.

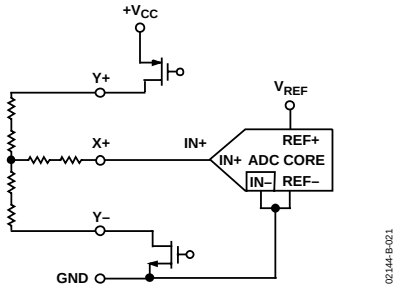


Figure 21. Single-Ended Reference Mode (SER/$\overline{DFR}$ = 1)

In this mode of operation, therefore, some voltage is likely to be lost across the internal switches and, in addition to this, it is unlikely that the internal switch resistance will track the resistance of the touch screen over temperature and supply, providing an additional source of error.

The alternative to this situation is to set the SER/$\overline{DFR}$ bit low. If one again considers making a Y-coordinate measurement, but now the +REF and −REF nodes of the ADC are connected directly to the Y+ and Y− pins, this means the analog-to-digital conversion is ratiometric. The result of the conversion is always a percentage of the external resistance, independent of how it could change with respect to the on resistance of the internal switches. Figure 22 shows the configuration for a ratiometric Y-coordinate measurement. It should be noted that the differential reference mode can be used only with $+V_{CC}$ since the source of the +REF voltage and cannot be used with V_{REF}.

The disadvantage of this mode of operation is that during both the acquisition phase and conversion process, the external touch screen must remain powered. This results in additional supply current for the duration of the conversion.

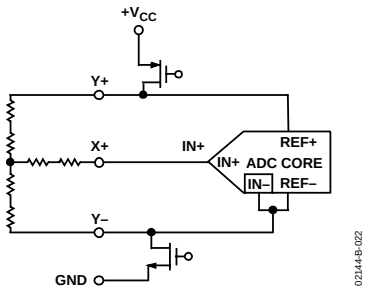


Figure 22. Differential Reference Mode (SER/$\overline{DFR}$ = 0)

CONTROL REGISTER

The control word provided to the ADC via the DIN pin is shown in Table 6. This provides the conversion start, channel addressing, ADC conversion resolution, configuration, and power-down of the AD7843.

Table 6 provides detailed information on the order and description of these control bits within the control word.

Initiate START

The first bit, the S bit, must always be set to 1 to initiate the start of the control word. The AD7843 ignores any inputs on the DIN line until the START bit is detected.

Channel Addressing

The next three bits in the control register, A2, A1, and A0, select the active input channel(s) of the input multiplexer (see Table 5 and Figure 19), touch screen drivers, and the reference inputs.

MODE

The MODE bit sets the resolution of the analog to digital converter. With 0 in this bit, the following conversion has 12 bits of resolution. With 1 in this bit, the following conversion has 8 bits of resolution.

SER/$\overline{DFR}$

The SER/$\overline{DFR}$ bit controls the reference mode, which can be either single-ended or differential if 1 or 0 is written to this bit, respectively. The differential mode is also referred to as the ratiometric conversion mode. This mode is optimum for X-position and Y-position measurements. The reference is derived from the voltage at the switch drivers, which is almost the same as the voltage to the touch screen. In this case, a separate reference voltage is not needed because the reference voltage to the ADC is the voltage across the touch screen. In single-ended mode, the reference voltage to the converter is always the difference between the V_{REF} and GND pins. See Table 5 and Figure 19 through Figure 22 for further information.

Because the supply current required by the device is so low, a precision reference can be used as the supply source to the AD7843. It may also be necessary to power the touch screen from the reference, which could require 5 mA to 10 mA. A REF19x voltage reference can source up to 30 mA and, as such, could supply both the ADC and the touch screen. Care must be taken, however, to ensure that the input voltage applied to the ADC does not exceed the reference voltage and therefore the supply voltage. See the Absolute Maximum Ratings section.

Note that the differential mode can only be used for X-position and Y-Position measurements. All other measurements require single-ended mode.

PD0 and PD1

The power management options are selected by programming the power management bits, PD0 and PD1, in the control register. Table 7 summarizes the available options. On power-up, PD0 defaults to 0, while PD1 defaults to 1..

Table 6. Control Register Bit Function Description

MSB							LSB
S	A2	A1	A0	MODE	SER/$\overline{DFR}$	PD1	PD0

Bit	Mnemonic	Comment
7	S	Start Bit. The control word starts with the first high bit on DIN. A new control word can start every 15th DCLK cycle when in the 12-bit conversion mode, or every 11th DCLK cycle when in 8-bit conversion mode.
6–4	A2–A0	Channel Select Bits. These three address bits, along with the SER/$\overline{DFR}$ bit, control the setting of the multiplexer input, switches, and reference inputs, as described in Table 5.
3	MODE	12-Bit/8-Bit Conversion Select Bit. This bit controls the resolution of the following conversion. With 0 in this bit, the conversion has a 12-bit resolution, or with 1 in this bit, the conversion has a 8-bit resolution.
2	SER/$\overline{DFR}$	Single-Ended/Differential Reference Select Bit. Along with Bits A2–A0, this bit controls the setting of the multiplexer input, switches, and reference inputs, as described in Table 5.
1, 0	PD1, PD0	Power Management Bits. These two bits decode the power-down mode of the AD7843, as shown in Table 7.

POWER VS. THROUGHPUT RATE

By using the power-down options on the AD7843 when not converting, the average power consumption of the device decreases at lower throughput rates. Figure 23 shows how, as the throughput rate is reduced while maintaining the DCLK frequency at 2 MHz, the device remains in its power-down state longer and the average current consumption over time drops accordingly.

For example, if the AD7843 is operated in a 24 DCLK continuous sampling mode, with a throughput rate of 10 kSPS and a SCLK of 2 MHz, and the device is placed in the power-down mode between conversions, (PD0, PD1 = 0, 0), the current consumption is calculated as follows. The power dissipation during normal operation is typically 210 μA (V_{CC} = 2.7 V). The power-up time of the ADC is instantaneous, so when the part is converting, it consumes 210 μA. In this mode of operation, the part powers up on the fourth falling edge of DCLK after the start bit is recognized. It goes back into power-down at the end of conversion on the 20th falling edge of DCLK. This means the part consumes 210 μA for 16 DCLK cycles only, 8 μs, during each conversion cycle. With a throughput rate of 10 kSPS, the cycle time is 100 μs and the average power dissipated during each cycle is (8/100) × (210 μA) = 16.8 μA.

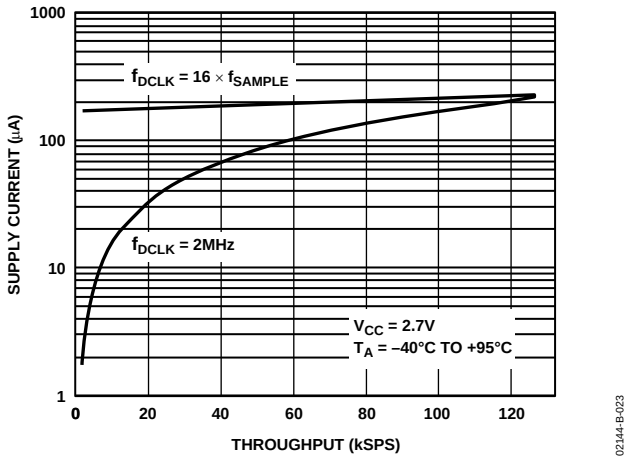


Figure 23. Supply Current vs. Throughput (μA)

Table 7. Power Management Options

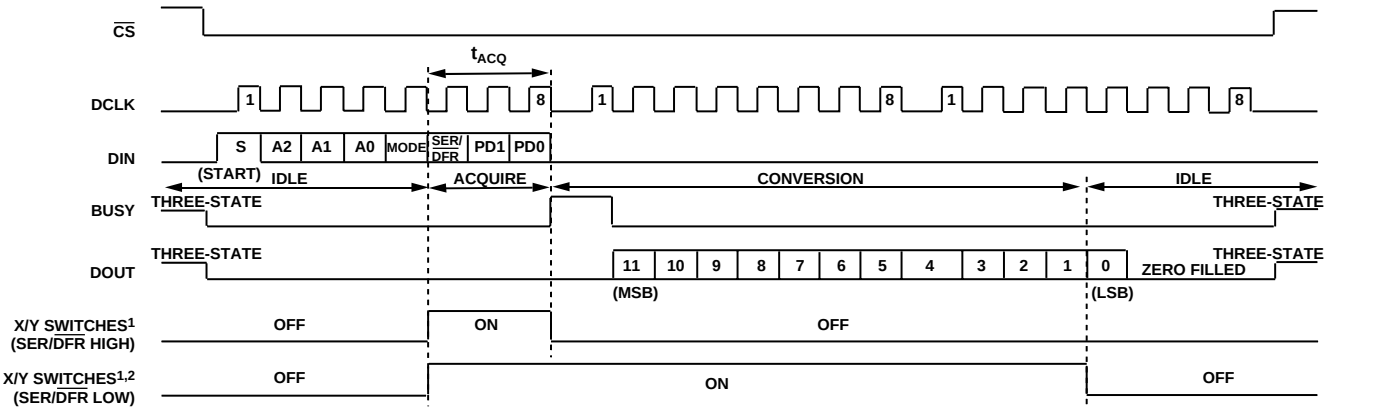
PD1	PD0	$\overline{\text{PENIRQ}}$	Description
0	0	Enabled	This configuration results in power-down of the device between conversions. The AD7843 only powers down between conversions. Once PD1 and PD0 are set to 0, 0, the conversion is performed first, and the AD7843 powers down upon completion of that conversion. At the start of the next conversion, the ADC instantly powers up to full power. This means there is no need for additional delays to ensure full operation, and the very first conversion is valid. The Y– switch is on while in power-down.
0	1	Disabled	This configuration results in the same behavior as when PD1 and PD0 have been programmed with 0, 0, except that $\overline{\text{PENIRQ}}$ is disabled. The Y– switch is off while in power-down.
1	0	Enabled	This configuration results in keeping the AD7843 permanently powered up with $\overline{\text{PENIRQ}}$ enabled.
1	1	Disabled	This configuration results in keeping the AD7843 always powered up with $\overline{\text{PENIRQ}}$ disabled.

SERIAL INTERFACE

Figure 24 shows the typical operation of the serial interface of the AD7843. The serial clock provides the conversion clock and also controls the transfer of information to and from the AD7843. One complete conversion can be achieved with 24 DCLK cycles.

The $\overline{CS}$ signal initiates the data transfer and conversion process. The falling edge of $\overline{CS}$ takes the BUSY output and the serial bus out of three-state. The first eight DCLK cycles are used to write to the control register via the DIN pin. The control register is updated in stages as each bit is clocked in. Once the converter has enough information about the following conversion to set the input multiplexer and switches appropriately, the converter enters acquisition mode and, if required, the internal switches are turned on. During the acquisition mode, the reference input data is updated. After the three DCLK cycles of acquisition, the control word is complete (the power management bits are now updated) and the converter enters conversion mode. At this point, track-and-hold goes into hold mode, the input signal is sampled, and the BUSY output goes high (BUSY returns low on the next falling edge of DCLK). The internal switches may also turn off at this point if in single-ended mode.

The next 12 DCLK cycles are used to perform the conversion and to clock out the conversion result. If the conversion is ratiometric (SER/$\overline{DFR}$ set low), the internal switches are on during the conversion. A 13th DCLK cycle is needed to allow the DSP/microcontroller to clock in the LSB. Three more DCLK cycles clock out the three trailing zeroes and complete the 24 DCLK transfer. The 24 DCLK cycles can be provided from a DSP or via three bursts of 8 clock cycles from a microcontroller.



NOTES
[1]Y DRIVERS ARE ON WHEN X+ IS SELECTED INPUT CHANNEL (A2–A0 = 001); X DRIVERS ARE ON WHEN Y+ IS SELECTED INPUT CHANNEL (A2–A0 = 101). WHEN PD1, PD0 = 10 OR 00, Y– WILL TURN ON AT THE END OF THE CONVERSION.
[2]DRIVERS WILL REMAIN ON IF POWER-DOWN MODE IS 11 (NO POWER-DOWN) UNTIL SELECTED INPUT CHANNEL, REFERENCE MODE, OR POWER-DOWN MODE IS CHANGED.

02144-B-024

Figure 24. Conversion Timing, 24 DCLKS per Conversion Cycle, 8-Bit Bus Interface. No DCLK delay required with dedicated serial port.

DETAILED SERIAL INTERFACE TIMING

Figure 25 shows the detailed timing diagram for serial interfacing to the AD7843. Writing information to the control register takes place on the first eight rising edges of DCLK in a data transfer. The control register is written to only if a START bit is detected (see the Control Register section) on DIN. The initiation of the following conversion also depends on the presence of the START bit. Throughout the eight DCLK cycles when data is being written to the part, the DOUT line is driven low. The MSB of the conversion result is clocked out on the falling edge of the ninth DCLK cycle and is valid on the rising edge of the tenth DCLK cycle; therefore, nine leading zeros can be clocked out prior to the MSB. This means the data seen on the DOUT line in the 24 DCLK conversion cycle is presented in the form of nine leading zeros, twelve bits of data, and three trailing zeros.

The rising edge of $\overline{CS}$ puts the bus and the BUSY output back into three-state, the DIN line is ignored, and, if a conversion is in progress at the time, this is also aborted. However, if $\overline{CS}$ is not brought high after the completion of the conversion cycle, then the part waits for the next START bit to initiate the next conversion. This means that each conversion does not necessarily need to be framed by $\overline{CS}$, because once $\overline{CS}$ goes low, the part detects each START bit and clocks in the control word after it on DIN. When the AD7843 is in the 12-bit conversion mode, a second START bit is not detected until seven DCLK pulses have elapsed after a control word is clocked in on DIN, that is, another START bit can be clocked in on the eighth DCLK rising edge after a control word is written to the device (see the Fifteen Clocks per Cycle section). If the device is in the 8-bit conversion mode, a second START bit is not recognized until three DCLK pulses elapse after the control word is clocked in, that is, another START bit can be clocked in on the fourth DCLK rising edge after a control word is written to the device.

Because a START bit can be recognized during a conversion, the control word for the next conversion can be clocked in during the current conversion, enabling the AD7843 to complete a conversion cycle in less than 24 DCLKs.

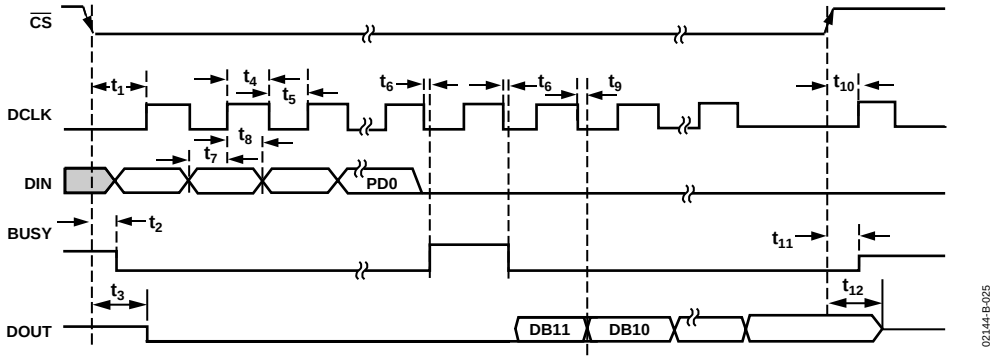


Figure 25. Detailed Timing Diagram

Sixteen Clocks per Cycle

The control bits for the next conversion can be overlapped with the current conversion to allow for a conversion every 16 DCLK cycles, as shown in Figure 26. This timing diagram also allows for the possibility of communication with other serial peripherals between each (eight DCLK) byte transfer between the processor and the converter. However, the conversion must be completed within a short enough time frame to avoid capacitive droop effects that could distort the conversion result. It should also be noted that the AD7843 is fully powered while other serial communications are taking place between byte transfers.

Fifteen Clocks per Cycle

Figure 27 shows the fastest way to clock the AD7843. This scheme does not work with most microcontrollers or DSPs because, in general, they are not capable of generating a 15-clock-cycle-per-serial transfer. However, some DSPs allow the number of clocks per cycle to be programmed; this method could also be used with FPGAs (field programmable gate arrays) or ASICs (application specific integrated circuits). As in the 16-clocks-per-cycle case, the control bits for the next conversion are overlapped with the current conversion to allow a conversion every 15 DCLK cycles, using 12 DCLKs to perform the conversion and three DCLKs to acquire the analog input. This effectively increases the throughput rate of the AD7843 beyond that used for the specifications that are tested using 16 DCLKs per cycle, and DCLK = 2 MHz.

8-Bit Conversion

By setting the MODE bit to 1 in the control register, the AD7843 can operate in 8-bit rather than 12-bit mode. This mode allows a faster throughput rate to be achieved, assuming 8-bit resolution is sufficient. When using the 8-bit mode, a conversion is complete four clock cycles earlier than in the 12-bit mode. This could be used with serial interfaces that provide 12 clock transfers, or two conversions could be completed with three 8-clock transfers. The throughput rate increases by 25% as a result of the shorter conversion cycle, but the conversion itself can occur at a faster clock rate because the internal settling time of the AD7843 is not as critical because settling to 8 bits is all that is required. The clock rate can be as much as 50% faster. The faster clock rate and fewer clock cycles combine to provide double the conversion rate.

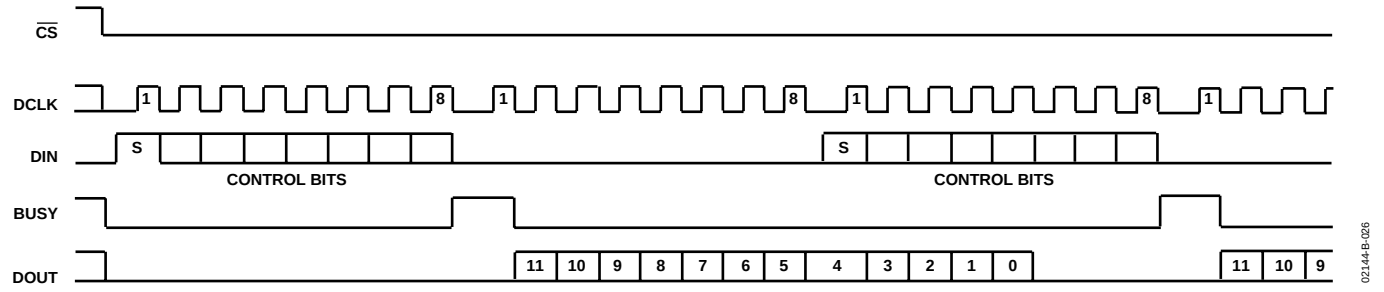


Figure 26. Conversion Timing, 16 DCLKS per Cycle, 8-Bit Bus Interface. No DCLK delay required with dedicated serial port.

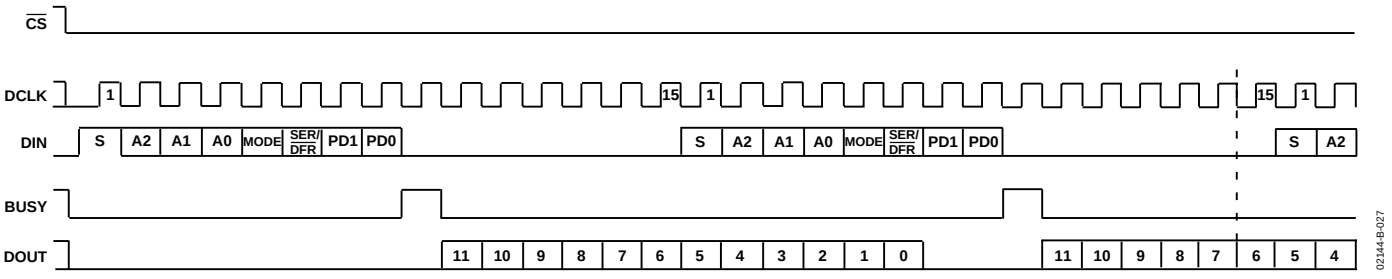


Figure 27. Conversion Timing, 15 DCLKS per Cycle, Maximum Throughput Rate

PEN INTERRUPT REQUEST

The pen interrupt equivalent output circuitry is outlined in Figure 28. By connecting a pull-up resistor (10 kΩ to 100 kΩ) between V_{CC} and this CMOS logic open-drain output, the $\overline{\text{PENIRQ}}$ output remains high normally. If $\overline{\text{PENIRQ}}$ is enabled (see Table 7), when the touch screen connected to the AD7843 is touched via a pen or finger, the $\overline{\text{PENIRQ}}$ output goes low, initiating an interrupt to a microprocessor that can then instruct a control word to be written to the AD7843 to initiate a conversion. This output can also be enabled between conversions during power-down (see Table 7), allowing power-up to be initiated only when the screen is touched. The result of the first touch screen coordinate conversion after power-up is valid, assuming any external reference is settled to the 12- or 8-bit level as required.

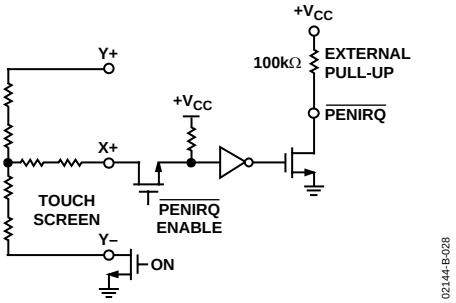


Figure 28. $\overline{\text{PENIRQ}}$ Functional Block Diagram

Figure 29 assumes that the $\overline{\text{PENIRQ}}$ function is enabled in the last write or that the part has just been powered up, so $\overline{\text{PENIRQ}}$ is enabled by default. Once the screen is touched, the $\overline{\text{PENIRQ}}$ output goes low a time t_{PEN} later. This delay is approximately 5 µs, assuming a 10 nF touch screen capacitance, and varies with the touch screen resistance actually used.

Once the START bit is detected, the pen interrupt function is disabled and the $\overline{\text{PENIRQ}}$ cannot respond to screen touches. The $\overline{\text{PENIRQ}}$ output remains low until the fourth falling edge of DCLK after the START bit has been clocked in, at which point it returns high as soon as possible, regardless of the touch screen capacitance. This does not mean that the pen interrupt function is now enabled again because the power-down bits have not yet been loaded to the control register. Regardless of whether $\overline{\text{PENIRQ}}$ is to be enabled again or not, the $\overline{\text{PENIRQ}}$ output normally always idles high. Assuming that the $\overline{\text{PENIRQ}}$ is enabled again as shown in Figure 29, once the conversion is complete, the $\overline{\text{PENIRQ}}$ output responds to a screen touch again.

The fact that $\overline{\text{PENIRQ}}$ returns high almost immediately after the fourth falling edge of DCLK means the user avoids any spurious interrupts on the microprocessor or DSP, which could occur if the interrupt request line on the microprocessor/DSP was unmasked during or toward the end of conversion with the $\overline{\text{PENIRQ}}$ pin still low. Once the next START bit is detected by the AD7843, the $\overline{\text{PENIRQ}}$ function is disabled again.

If the control register write operation overlaps with the data read, a START bit is always detected prior to the end of conversion. This means that even if the $\overline{\text{PENIRQ}}$ function has been enabled in the control register, it is disabled by the START bit again before the end of the conversion is reached; therefore the $\overline{\text{PENIRQ}}$ function effectively cannot be used in this mode. However, as conversions are occurring continuously, the $\overline{\text{PENIRQ}}$ function is not necessary and, therefore, redundant.

GROUNDING AND LAYOUT

For information on grounding and layout considerations for the AD7843, refer to Application Note AN-577, Layout and Grounding Recommendations for Touch Screen Digitizers.

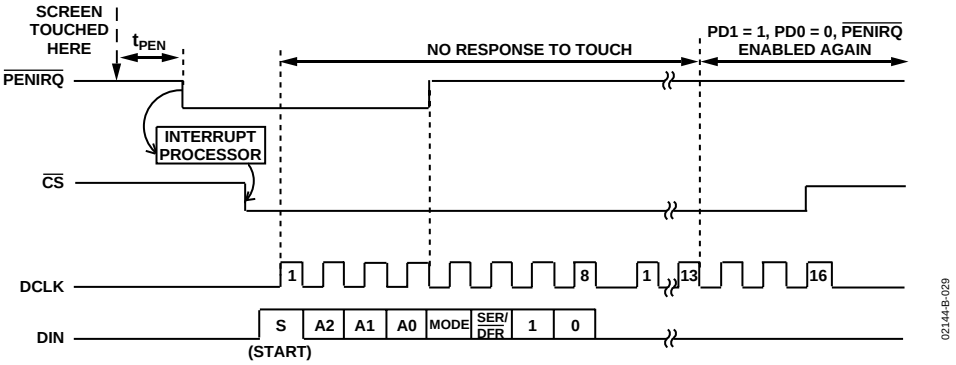


Figure 29. $\overline{\text{PENIRQ}}$ Timing Diagram

OUTLINE DIMENSIONS

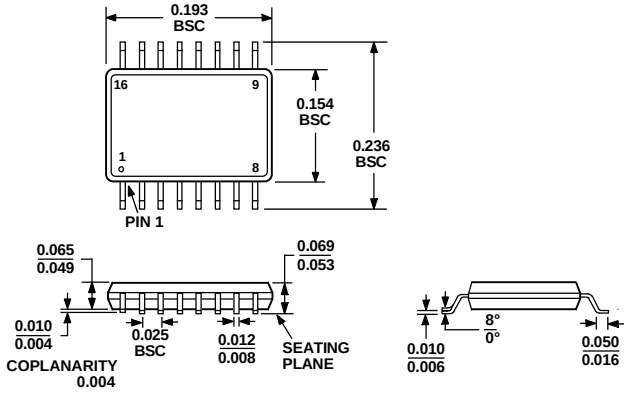


Figure 30. 16-Lead Shrink Small Outline Package [QSOP]
(RQ-16)
Dimensions shown in inches

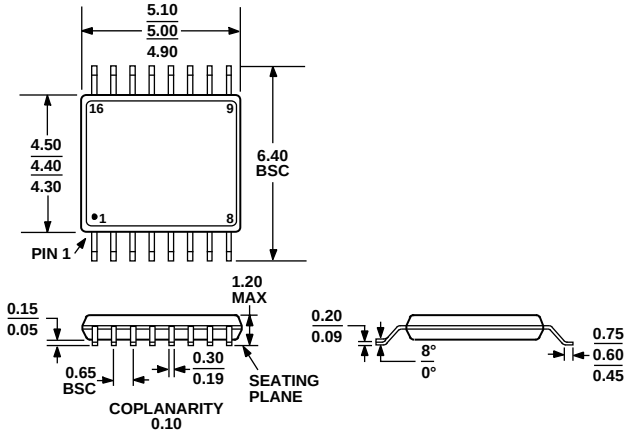


Figure 31. 16-Lead Thin Shrink Small Outline Package [TSSOP]
(RU-16)
Dimensions shown in millimeters

ORDERING GUIDE

Model	Temperature Range	Linearity Error (LSB)[1]	Package Description	Package Option
AD7843ARQ	−40°C to +85°C	±2	QSOP	RQ-16
AD7843ARQ-REEL	−40°C to +85°C	±2	QSOP	RQ-16
AD7843ARQ-REEL7	−40°C to +85°C	±2	QSOP	RQ-16
AD7843ARQZ[2]	−40°C to +85°C	±2	QSOP	RQ-16
AD7843ARQZ-REEL[2]	−40°C to +85°C	±2	QSOP	RQ-16
AD7843ARQZ-REEL7[2]	−40°C to +85°C	±2	QSOP	RQ-16
AD7843ARU	−40°C to +85°C	±2	TSSOP	RU-16
AD7843ARU-REEL	−40°C to +85°C	±2	TSSOP	RU-16
AD7843ARU-REEL7	−40°C to +85°C	±2	TSSOP	RU-16
EVAL-AD7843CB[3]			Evaluation Board	
EVAL-CONTROL BRD2[4]			Controller Board	

[1] Linearity error here refers to integral linearity error.
[2] Z = Pb-free part. Pb-free parts are branded with a # before the date code.
[3] This can be used as a stand-alone evaluation board, or in conjunction with the Evaluation Board Controller for evaluation/demonstration purposes.
[4] This Evaluation Board Controller is a complete unit allowing a PC to control and communicate with all Analog Devices evaluation boards ending in the CB designator.

C02144–0–3/04(B)